to or disclaimer of the subject matter therein. New claims 11-17 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and they be withdrawn.

Rejections Under 35 U.S.C. § 102

Claim 10 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,259,881 to Edwards, et al. ("Edwards"). This rejection is mooted by the cancellation of claim 10.

Claim 10 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,512,320 to Turner, et al. ("Turner"). This rejection is mooted by the cancellation of claim 10.

Claim 10 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,013,162 to Kobayashi, et al. ("Kobayashi"). This rejection is mooted by the cancellation of claim 10.

Other Matters

New claims 11-17 have been added. These claims are fully supported by the specification, and neither Edwards, Turner, Kobayashi, nor other prior of record teach or suggest all of the claimed features. Accordingly, claims 11-17 should be allowed.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**."

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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Date: January 14, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 10 has been cancelled.

Please add new claims 11-17, as follows:

(New) 11. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire including a plurality of gate lines formed on the insulating substrate and a plurality of gate electrodes connected to the gate lines;

a gate insulating layer formed on the gate wire;

a plurality of data lines crossing the gate lines formed on the gate insulating layer and made of an amorphous silicon layer, a doped amorphous silicon layer, and a metal layer;

a plurality of channel portions made of the amorphous silicon layer and formed on the gate insulating layer over the gate electrode;

a plurality of source electrodes connected to the data lines wherein at least a portion of the source electrodes are formed on the channel portions;

a plurality of drain electrodes facing the source electrode on the channel portion;

a passivation layer covering the data lines, the channel portions, and the gate insulating layer, having a plurality of contact holes exposing at least a portion of the drain electrodes; and

a plurality of pixel electrodes formed on the passivation layer and connected to the drain electrode through the contact holes.

(New) 12. The thin film transistor array panel of claim 11, wherein the amorphous silicon layer of the data lines has at least a portion of the amorphous silicon layer located within the border line of the metal layer of the data lines.

(New) 13. The thin film transistor array panel of claim 12, wherein the width of the metal layer is wider than that of the amorphous silicon layer where the amorphous silicon layer of the data lines is located within the border line of the metal layer of the data lines.

(New) 14. The thin film transistor array panel of claim 11, wherein the source electrodes and the drain electrodes are made of the doped amorphous layer and the metal layer.

(New) 15. The thin film transistor array panel of claim 11, wherein the gate wire has a double layered structure made out of a first metal layer, which is made of one of Al and Al-Nd, and a second metal layer which is made of one of Mo, Ta, Cr and their alloys.

(New) 16. The thin film transistor array panel of claim 15, wherein the metal layer of the data lines, the source electrodes, and the drain electrodes are made of Cr.

(New) 17. The thin film transistor array panel of claim 11, wherein the pixel electrodes are made of indium tin oxide (ITO). --